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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PROCTOR, JASON SCOTT	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/829,535	HSU ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-24 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 09 April 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: There are numerous errors related to drawing references. Some examples include "OR gates 14-16" (paragraph 00002, lines 5-6) where FIG. 1 has no element 16; "The waveform data 28 simulator 32" (paragraph 00005, lines 13-14) where the circuit simulator of FIG. 3 is element 23; and "vertical scroll bar 51 (step 80)" (paragraph 00061, line 2) where the step is element 180. See MPEP 608.02(e).

Appropriate correction is required.

2. The disclosure is objected to because of the following informalities: In several instances, the specification does not correspond to the drawings. Some examples include "R4 box 57 of FIG. 7" (paragraph 00040, line 1) where the drawing and specification suggest R3 box 55 (FIG. 8; paragraph 00040, lines 1-12); "signal transitioned from high to low" (paragraph 00037, lines 2-3) where FIG. 4 and the disclosure (paragraph 00008, lines 10-13) indicate the signal transitioned from low to high; and "when the CLK1 signal clocked registers 21 and 22" (paragraph 00008, lines 25-26) where the registers involved appear to be 20 and 21. See MPEP 608.02(e).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Watkins et al.

5. Regarding claim 1, Watkins et al. teaches a system which aids in the design and simulation of digital logic circuits wherein

the logic model is processed to produce waveform data indicating the states of circuit elements as a function of time (FIG. 4, elements 410, 412, 414, 416, 418, and 420; column 2, lines 5-21),

the system provides features that allow for certain elements to be "activated" or "deactivated" (column 8, lines 50-53; column 10, lines 5-12) in successive simulations, the result of which is a plurality circuit models that depict the circuit inputs and circuit elements which influence the output of a given register, and

the system generates a display including several register symbols (FIG. 3, element 320; FIG. 4, element 320; column 8, lines 1-6; column 7, lines 48-57) also including a representation of the logical relationship depicted by at least one of the net models (FIG. 3, all elements except 300, 310, 314,

318, 320, 330, and 322; FIG. 4, all elements except 400, 410, 412, 414, 416, 418, 420, 318, 320, and 322).

6. Regarding claim 13, Watkins et al. teaches an apparatus which aids in the design and simulation of digital logic circuits comprising

a logic compiler, a logic simulator, and a logic verifier (column 5, lines 59-61) which simulate the behavior of the circuit model to thereby produce waveform data (column 2, lines 5-21; column 7, lines 12-16) indicating the states of circuit input and register output signals as functions of time (column 7, lines 16-19; column 7, lines 36-47; column 8, lines 3-6; FIG. 4),

means for processing the logic model to generate a plurality of net models (column 8, lines 50-54; column 10, lines 5-12) which can be configured to correspond to a separate register and to depict the relationship between the signals that influence the register's input signal between clock signal edges, and

means for generating a display including a plurality of register symbols (FIG. 4, elements 302, 304, 306, and 320) and register state symbols (FIG. 4, element 322) indicating the state of a corresponding register output signal after being receiving a clock signal (FIG. 4, element 336 corresponding to "CP"; column 7, lines 41-57) as indicated by waveform data (FIG. 4, elements 410, 412, 414, 416, 418, and 420) wherein the display also includes a representation of a logical relationship depicted by at least one

of the net models (FIG. 4, all elements except 400, 410, 412, 414, 416, 418, 420, 318, 320, and 322).

7. Regarding claims 2 and 14, Watkins et al. teaches a system wherein the data elements (FIG. 3, element 322) corresponding to the register symbols (FIG. 3, element 320) are arranged in the display to indicate the timing of clock signals (column 5, lines 17-20; column 7, lines 48-57).

8. Regarding claims 3 and 15 Watkins et al. teaches a system wherein the state tables (FIG. 3, element 320; FIG. 4, element 320) and circuit schematics (FIG. 3, all elements except 300, 310, 314, 318, 320, 330, and 322; FIG. 4, all elements except 400, 410, 412, 414, 416, 418, 420, 318, 320, and 322) are displayed concurrently (FIG. 3; FIG. 4) indicating that the state of a given register is the logical function of one or more outputs from other registers represented by the register symbols (FIG. 3, element 320) in the state tables (FIG. 3, element 318).

9. Regarding claim 4, Watkins et al. teaches a system wherein the display includes input signal symbols (FIG. 3, element 320, "CD") and input signal state symbols (FIG. 3, element 322, the column below "CD" of element 320) depicting the state of input signals at separate times during the simulation (column 7, lines 48-57).

10. Regarding claim 5, Watkins et al. teaches a system wherein the display, including input signal symbols (FIG. 3, element 320, "CD"; FIG. 3, element 322, the column below "CD" of element 320), is arranged such that the symbols depict the state of the input signals at separate times (column 7, lines 48-57).

11. Regarding claim 6, Watkins et al. teaches a system wherein the state tables (FIG. 3, element 320; FIG. 4, element 320) and circuit schematics (FIG. 3, all elements except 300, 310, 314, 318, 320, 330, and 322; FIG. 4, all elements except 400, 410, 412, 414, 416, 418, 420, 318, 320, and 322) are displayed together (FIG. 3; FIG. 4) indicating that the state of a given register (FIG. 3, element 306) is the logical function of one or more outputs from other registers (FIG. 3, element 330) and the state of an input signal (FIG. 3, element 334) represented by the register symbols (FIG. 3, element 320) in the state tables (FIG. 3, element 318).

12. Regarding claims 7 and 19, Watkins et al. teaches a system wherein the logical relationship between registers (FIG. 3, elements 302, 304, and 306) is represented using lines (FIG. 3, elements 324 and 312) each connected to two of the register symbols.

13. Regarding claims 8 and 20, Watkins et al. teaches a system wherein the logical relationship between registers and inputs comprises a graphical representation of the net models (FIG. 3, all elements except 300, 310, 314, 318, 320, 330, and 322; FIG. 4, all elements except 400, 410, 412, 414, 416, 418, 420, 318, 320, and 322) linking the registers (FIG. 3, element 320; FIG. 4, element 320).

14. Regarding claim 9, Watkins et al. teaches a system wherein register symbols (FIG. 3, elements 302 and 304) are each connected to a second register (FIG. 3, elements 304 and 306, respectively) by a line (FIG. 3, elements 324 and 312, respectively) and connected to an input signal symbol (FIG. 3, "CD") by another line (FIG. 3, element 334).

15. Regarding claim 10, Watkins et al. teaches a system wherein the representation of a logical relationship comprises a graphical representation of a net model (FIG. 4 all elements except 400, 410, 412, 414, 416, 418, 420, 318, 320, and 322) wherein the graphical representation indicates how an input signal state (FIG. 4, element 420 corresponding to input signal element 334) corresponding to an input signal symbol (FIG. 4, "CD") logically influences a state of a register input signal (FIG. 4, "CD" within element 304) corresponding to a displayed register symbol (FIG. 4, element 304).

16. Regarding claim 11, Watkins et al. teaches a system wherein the register state symbols and input signal state symbols (FIG. 3, element 322) are positioned in the display to represent the time at which the registers and input signals are in the depicted states.

17. Regarding claim 12, Watkins et al. teaches a method which aids in the design and simulation of digital logic circuits comprising

displaying a plurality of register symbols (FIG. 4, elements 302, 304, 306, and 320) and register state symbols (FIG. 4, element 322) indicating a state of a register after receiving a clock signal (FIG. 4, element 336) as indicated by waveform data (FIG. 4, element 418), wherein the position of the register state symbols represents a time occurrence of a clocked pulse signal edge,

displaying a plurality of input signal symbols (FIG. 4, elements 334, 336, and 320) and input signal state symbols (FIG. 4, elements 322) which indicate

a state of the input signal at separate times represented by the position of the input signal state symbols, and

displaying a representation of logic (FIG. 4, all elements except 400, 410, 412, 414, 416, 418, 420, 318, 320, and 322) interconnecting register symbols (FIG. 4, elements 302, 304, and 306) and input signal symbols (FIG. 4, element 336 corresponding to "CP" and element 334 corresponding to "CD") indicating how states of the input signals and register output signals influence states of register input signals.

18. Regarding claim 16, Watkins et al. teaches a system wherein the display includes input signal symbols (FIG. 3, element 320, "CD"; FIG. 3, element 322, the column below "CD" of element 320) depicting the state of input signals at separate times during the simulation (column 7, lines 48-57).

19. Regarding claim 17, Watkins et al. teaches a system wherein the display, including input signal symbols (FIG. 3, element 320, "CD"; FIG. 3, element 322, the column below "CD" of element 320), arranges the symbols such that they depict the state of the input signals at separate times (column 7, lines 48-57).

20. Regarding claim 18, Watkins et al. teaches a system wherein the state tables (FIG. 3, element 320; FIG. 4, element 320) and circuit schematics (FIG. 3, all elements except 300, 318, 320, and 322) are displayed together (FIG. 3; FIG. 4) indicating that the state of a given register (FIG. 3, element 306) is the logical function of one or more outputs from other registers (FIG. 3, element 330) and the state of an input signal (FIG.

3, element 334) represented by the register symbols (FIG. 3, element 320) in the state tables (FIG. 3, element 318).

21. Regarding claim 21, Watkins et al. teaches a system wherein register symbols (FIG. 3, elements 302 and 304) are each connected to a second register (FIG. 3, elements 304 and 306, respectively) by a line (FIG. 3, elements 324 and 312, respectively) and connected to an input signal symbol (FIG. 3, "CD") by another line (FIG. 3, element 334).

22. Regarding claim 22, Watkins et al. teaches a system wherein the representation of a logical relationship comprises a graphical representation of a net model (FIG. 4 all elements except 400, 410, 412, 414, 416, 418, 420, 318, 320, and 322) wherein the graphical representation indicates how an input signal state (FIG. 4, element 420 corresponding to input signal element 334) corresponding to an input signal symbol (FIG. 4, "CD") logically influences a state of a register input signal (FIG. 4, "CD" within element 304) corresponding to a displayed register symbol (FIG. 4, element 304).

23. Regarding claim 23, Watkins et al. teaches a system wherein the register state symbols and input signal state symbols (FIG. 3, element 322) are positioned in the display to represent the time at which the registers and input signals are in the depicted states.

24. Regarding claim 24, Watkins et al. teaches an apparatus comprising

a logic compiler, a logic simulator, and a logic verifier (column 5, lines 59-61) which simulate the behavior of the circuit model (column 7, lines 12-16) to thereby produce waveform data indicating the states of circuit input and

register output signals as functions of clock signal timing (column 7, lines 16-19; column 7, lines 36-47; column 8, lines 3-6; FIG. 4),

means for processing the logic model to produce waveform data corresponding to and displayed concurrently with the elements of the circuit schematic (column 8, lines 3-6; FIG. 4), thereby producing a model depicting the structure of the circuit as well as the behavior of the circuit as a function of time,

means for producing a display which uses separate symbols to represent successive circuit input and register output signal states relative to the clock signal during simulation (FIG. 4, element 318; column 7, lines 48-57), and

displays fan-in and fan-out relationships depicting the influence of the various circuit input and register output signals (FIG. 4, all elements except 400, 410, 412, 414, 416, 418, 420, 318, 320, and 322).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (703) 305-0542 or (571) 272-3713 beginning in October 2004. The examiner can normally be reached on 8am-4pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J Teska can be reached on (703) 305-9704 or (571) 272-3716

beginning in October 2004. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
Art Unit 2123

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